IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Attorney Docket Number 15138US02

In re Application of:	)	
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Pai	)	**Electronically Filed**
Serial No.: 10/736,125	)	
Filing Date: 12/15/2003	)	
Examiner: Tseng	)	
Confirmation No.: 3609	)	
Art Unit No. 2136	)	
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REQUEST FOR PRE-APPEAL REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This amendment is filed in response to the Office Action mailed 12/2/2008.

REMARKS

Claims 18-28 are presently pending and stand rejected. Assignee respectfully appeals the rejection and requests pre-appeal brief review of the rejections to claims 18 and 20-23 and 28. Claims 20-23 and 28 depend on claim 18. Claim 18 were rejected for double patenting and under 35 U.S.C. 102 as being anticipated by Lee.

Assignee presents Examiner with a terminal disclaimer to overcome the double-patenting rejection.

Claim 18 recites:

> A direct memory access controller, said direct memory access controller comprising:
>
> a state logic machine for receiving a single command to provide a specified range of a plurality of sequential data words; and
>
> a memory controller for fetching a first portion of the range and a second portion of the range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion, after the state logic receives the single command.

Examiner has indicated that Lee teaches "a state logic machine (fig. 4, state machine 404; and fig. 12, FSM 1206) for receiving a single command (fig. 5, control command 501; and fig. 6, command 601) to provide a specific range (col. 11, lines 15-19, address range of external memory to be accessed) of a plurality of sequential data words (col. 4, lines 24-29, accessed memory blocks has plurality of sequential data words)".

Assignee respectfully traverses the rejection because

Lee does not disclose "a state logic machine for receiving a single command". Although Examiner has indicated that Lee teaches "a state logic machine (fig. 4, state machine 404; and fig. 12, FSM 1206)", the "state machine 404" and "FSM 1206" do not receive commands. Rather, the "co-processor interface 402 interprets the coprocessor command data generated from RISC processor 207". It is noted that Examiner reads "single command" on Figure 5, control command 501, and Figure 6, Command 601. However, Fig. 5 and Fig 6 are views illustrating the coprocessor command sets used at the coprocessor interface 402." Thus, Lee does not disclose "a state logic machine for receiving a single command".

Additionally, Assignee argued in the response to the previous office action that commands "501 and 601 do not include the capability to specify a range of data words. See Col. 10, Line 59 - Col. 11, Line 36. Accordingly, Lee does not teach "a single command to provide a specified range of a plurality of sequential data words".

Examiner now indicates that Lee "discloses the command 601 contains fields such as CRd to select external memory as first range, internal DEC memory as second range, and local memory as third possible range". Examiner also makes citation to col. 11, lines 15-19.

Assignee respectfully traverses the rejection. It is first noted that command 501 is "used for reading or writing the register of each block included in VDEC 203". "CRn 505 represents the upper 4 bits of the register address to be used", "CRm represents the lower 4 bits of the register address to be used". The foregoing is not "a specified range of a plurality of sequential data words". Turning to command 601, CRd merely identifies which memory

is used. It appears from the Office Action that Examiner's position is that identification of a memory to be used is the specification of a range of addresses, the range being the first data word to the last data word of the identified memory. However, even if, arguendo, identification of a memory is held to be specification of a range being the first data word to the last data word of the identified memory, Assignee respectfully submits that Lee's identification of a memory, CRd is "a single command to provide" all of the words from the first data word of the identified memory to the last word of the identified memory.

Additionally, Assignee also traverses because the command 601 is not received by the VDEC 203, Lee teaches that VDEC 203 "should inform to RISC processor 207 by using a command 601, and then RISC processor 207 can access data through main bus 211." Col. 11, Lines 15-19. Thus, instead of VDEC 203 "receiving" the command 601, VDEC actually issues command 601 for the RISC processor 207.

Examiner has also indicated that Lee teaches "a memory controller (fig. 11, buffer controller 1113) for fetching a first portion (fig. 11, portion of VLD input buffer 1112) of the range and a second portion (fig. 11, portion of VLD input buffer 1112) of the range after fetching the first portion". Office Action at 8.

Assignee respectfully traverses the rejection because it is noted that "the range" takes antecedent basis from "a state logic machine for receiving a single command to provide a specified range of a plurality of sequential data words". However, even if arguendo, the specified range is "col. 11, lines 15-19, address range of external memory to be accessed", it is noted that the portions of the VLD

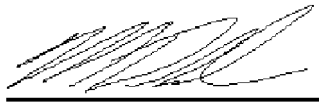
input buffer 1112 are not portions of "the range" specified by the single command. Accordingly, Assignee also traverses the rejection to claim 18 for this additional reason.

CONCLUSION

For at least the foregoing reasons, Assignee respectfully submits that each of the pending claims are allowable and Examiner is respectfully requested to pass this case to issuance. The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: March 2, 2009

Respectfully submitted,



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